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Bib Data Sheet

CONFIRMATION NO. 5589

SERIAL NUMBER 10/803,335	FILING DATE 03/17/2004 RULE	CLASS 716	GROUP ART UNIT 2825	ATTORNEY DOCKET NO. X-1039-1D US
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APPLICANTS

Peter H. Alfke, Los Altos Hills, CA;

Himanshu J. Verma, Mountain View, CA;

** CONTINUING DATA *YES HR* *****

This application is a DIV of 10/198,801 07/19/2002 PAT 6,734,703

** FOREIGN APPLICATIONS *NONE HR* *****

IF REQUIRED, FOREIGN FILING LICENSE GRANTED

** 05/31/2004

Foreign Priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	STATE OR COUNTRY CA	SHEETS DRAWING 6	TOTAL CLAIMS <i>18/14</i>	INDEPENDENT CLAIMS <i>2</i>
35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> Met after Allowance				
Verified and Acknowledged	Examiner's Signature <i>Aditya K. K. K. HR</i>	Initials <i>HR</i>		

ADDRESS

24309
 XILINX, INC
 ATTN: LEGAL DEPARTMENT
 2100 LOGIC DR
 SAN JOSE, CA
 95124

TITLE

Circuits and methods for analyzing timing characteristics of sequential logic elements

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